

## THERMAL STRESSES IN MICROELECTRONICS SUBASSEMBLIES: QUANTITATIVE CHARACTERIZATION USING PHOTOMECHANICS METHODS

**Bongtae Han**  
*CALCE Electronics Products and Systems Center  
Mechanical Engineering Department  
University of Maryland  
College Park, Maryland, USA*

*Several optical methods for in-situ displacement measurement are presented as a tool to characterize thermomechanical behavior of microelectronics subassemblies. Features and recent developments of the methods are reviewed and applications to diverse problems are illustrated to demonstrate wide applicability of the methods. The whole-field displacement information, with various sensitivity and resolution scales, is ideally suited for the deformation study of a broad range of problems in microelectronics packaging. The methods are mature and they can be practiced routinely. More applications are anticipated.*

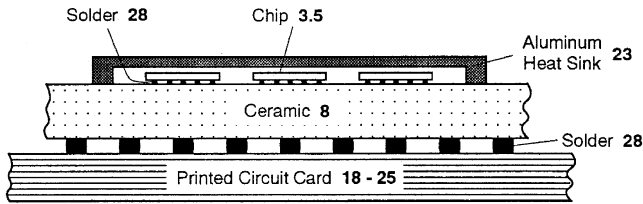
**Keywords** far infrared Fizeau interferometry, interconnections, microelectronics packaging, microscopic moiré interferometry, moiré interferometry, photomechanics methods, shadow moiré, Twyman/Green interferometry

A microelectronics subassembly is comprised of various conducting and insulating materials, which have different coefficients of thermal expansion (CTE) [1]. Figure 1 illustrates a cross-sectional view of a multichip ceramic ball grid array (CBGA) package assembly, where a silicon chip is mounted on a multilayer ceramic module and the module is attached to a printed circuit board (PCB) through solder ball interconnections to form a final second level assembly. In addition, a metal heat sink

This article was an invited lecture at the Fifth International Congress on Thermal Stresses, *Thermal Stresses 2003*, June 8–11, 2003, at Virginia Tech, Blacksburg, VA.

The author wishes to thank all the co-authors of the cited references for their contributions.

Address correspondence to Prof. Bongtae Han, CALCE Electronics Products and Systems Center, Mechanical Engineering Department, University of Maryland, College Park, MD 20742. E-mail: bthan@eng.umd.edu



**Figure 1.** Cross-sectional view of a multichip CBGA package assembly. The bold number indicates a typical CTE value of each material in ppm/°C [1].

is attached to the module to dissipate the excessive heat. The bold numbers shown in Figure 1 indicate a typical CTE value of each material in ppm/°C. When the chip is powered so that the assembly is subjected to a temperature change, each material deforms at a different rate. This nonuniform CTE distribution produces thermally induced mechanical stresses within the package assembly.

The thermal stresses are induced by (1) a global CTE mismatch between the module and the PCB and (2) a local CTE mismatch between the adjacent materials at the interfaces. The effect of global CTE mismatch is illustrated in Figure 2*a*. When the assembly is cooled from an assembly temperature, the PCB contracts more than the module by  $(\alpha_2 - \alpha_1) \times \text{DNP}_{\text{max}} \times \Delta T$ , where  $\alpha_1$  and  $\alpha_2$  are the CTE values of module and PCB, respectively,  $\text{DNP}_{\text{max}}$  is the maximum distance from the neutral point, and  $\Delta T$  is the temperature excursion. This uneven contraction produces a global bending of the whole assembly as well as relative horizontal displacements between the top and bottom of the solder interconnections. The effect of local CTE mismatch on the solder deformation is illustrated in Figure 2*b*, where the dashed line indicates the original shape of the solder joint at the reflow temperature. When it is cooled to room temperature, the free thermal contraction of the solder joint at the interfaces is constrained by adjacent materials, which have a lower CTE. This effect is highly localized near the interfaces.

In general, if the global effect reinforces the local effect at a point in the package, the concentrated strain will be accumulated during thermal cycles, which would result in the premature failure of the device during operation. Figure 3 shows the cross section of the leftmost solder ball of the CBGA package assembly before and after an accelerated thermal cycling (ATC) test. The relative horizontal displacements and fatigue cracks in the failed solder joint are evident.

In the past decades, numerous optical methods for deformation measurements have matured and emerged as important engineering tools [2, 3]. The methods provide whole-field displacement information with various sensitivities and resolutions. Recently, several methods have been applied to microelectronics product development. They include moiré interferometry [4–19], microscopic moiré interferometry [10, 12, 16, 20–22], Twyman/Green interferometry [12, 16, 23], shadow moiré [24–28], and far infrared Fizeau interferometry [29, 30]. The first two provide contour maps of in-plane displacement fields, and the next three map out-of-plane displacement fields. This article presents recent developments of the methods and illustrates selected applications.

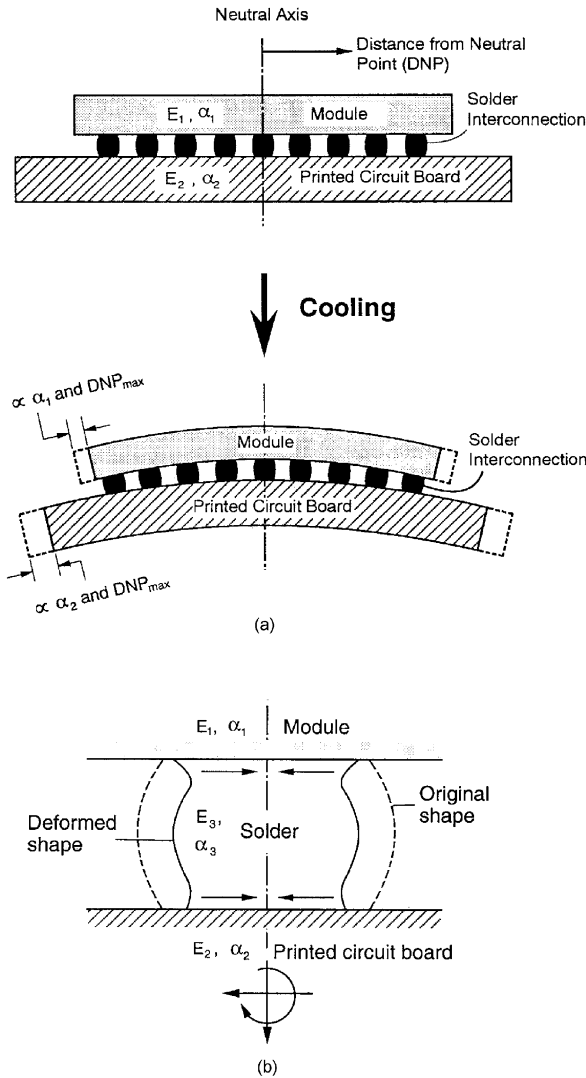
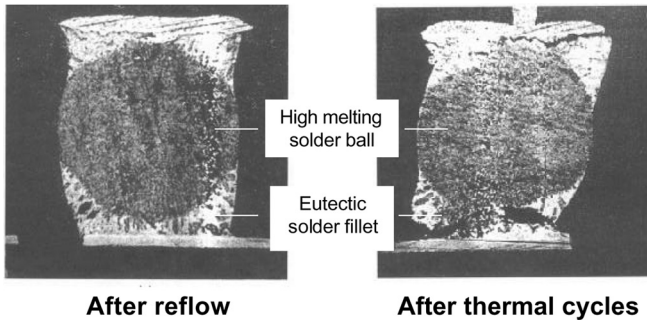


Figure 2. Schematic illustration of the effect of (a) global CTE mismatch and (b) local CTE mismatch [1].

## THERMAL STRAIN ANALYSIS BY MOIRÉ INTERFEROMETRY

### Basic Principle

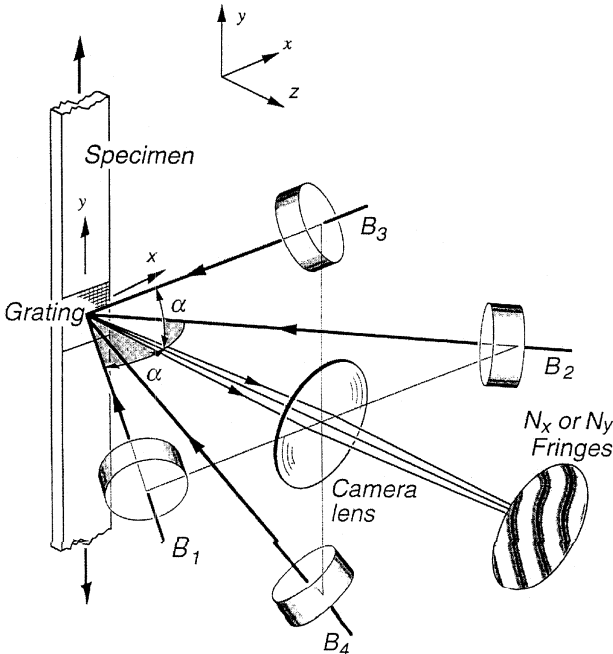
The general scheme of moiré interferometry is illustrated in Figure 4. A high-frequency cross-line grating on the specimen, initially of frequency  $f_s$ , deforms together with the specimen. A parallel (collimated) beam of laser light,  $B_1$  strikes the specimen and a portion is diffracted back, nominally perpendicular to the specimen, in the +1 diffraction order of the specimen grating. Light from the mutually coherent



**Figure 3.** Cross section of a solder ball of CBGA package assembly before and after an accelerated thermal cycling test [1].

collimated beam  $B_2$  is diffracted back in its  $-1$  order. Since the specimen grating is deformed as a result of the applied loads, these diffracted beams are no longer collimated. Instead, they are beams with warped wavefronts, where the warpages are related to the deformation of the grating. These two coherent beams interfere in the image plane of the camera lens, producing an interference pattern of dark and light bands, which is the  $N_x$  moiré pattern.

Similarly, mutually coherent collimated beams  $B_3$  and  $B_4$ , centered in the vertical plane, are diffracted in  $+1$  and  $-1$  diffraction orders by the nominally horizontal



**Figure 4.** Schematic illustration of four-beam moiré interferometry to record the  $N_x$  and  $N_y$  fringe patterns, which depict the  $U$  and  $V$  displacement fields [2].

lines of the deformed specimen grating. These two diffracted beams interfere to produce the  $N_y$  moiré pattern. In practice, beams  $B_1$  and  $B_2$  are blocked, so the  $N_y$  fringes are viewed alone. Alternately,  $B_3$  and  $B_4$  are blocked to view the  $N_x$  fringes.

These moiré patterns are contour maps of the  $U$  and  $V$  displacement fields, that is, the displacements in the  $x$ - and  $y$ -directions, respectively, of each point in the specimen grating. The relationships, for every  $x, y$  point in the field of view, are

$$U(x, y) = \frac{1}{2f_s} N_x(x, y) \quad V(x, y) = \frac{1}{2f_s} N_y(x, y) \quad (1)$$

In routine practice of moiré interferometry,  $f_s = 1,200$  lines/mm (30,480 lines/in.). In the fringe patterns, the contour interval is  $1/2f_s$ , which is  $0.417 \mu\text{m}$  displacement per fringe order. The sensitivity is its reciprocal, 2.4 fringes per micron displacement. For microscopic moiré interferometry, sensitivity of 57.6 fringe contours per micron displacement has been achieved.

### Extension: Microscopic Moiré Interferometry

Special considerations arise for deformation measurements of tiny specimens or tiny regions of larger specimens. The relative displacements within a small field of view will be small (even if the strains are not small), so the number of moiré fringes might not be enough for an accurate analysis. Perhaps the most important consideration, therefore, is the need for increased displacement sensitivity or enhanced sensitivity beyond the high sensitivity discussed previously.

In a method called *microscopic moiré interferometry*, sensitivity is increased progressively by two techniques. The first is an *immersion interferometer*, whereby the virtual reference grating is formed inside a medium of higher index of refraction; this strategy reduces the wavelength of the light and thus increases the upper limit of frequency for the virtual reference grating. Virtual reference gratings of 4,800 lines/mm (122,000 lines/in.) are produced in practice, thus doubling the usual basic sensitivity [31]. The second technique is optical/digital fringe multiplication (O/DFM), whereby fringe shifting and an efficient algorithm are used to generate an enhanced contour map of the displacement field; the map displays  $\beta$  times as many fringe contours as the original moiré pattern [32]. In practice,  $\beta = 12$  has been achieved for microscopic moiré interferometry, which, with the doubled sensitivity, represents a multiplication of 24.

A specific system is described briefly here but is described in much more detail in [2, 31]. The technique is based on the premise that the moiré pattern encompassing the small field of view will contain only a few fringes. Accordingly, it is practical to record the pattern by a CCD camera. Good fringe resolution is preserved because the pattern is recorded with numerous pixels per fringe.

The apparatus is illustrated in Figure 5. The specimen is coupled optically to the interferometer by a thin layer of immersion fluid so that beams corresponding to  $B_1, \dots, B_4$  in Figure 4 propagate in a refractive medium. A magnified view of the fringe pattern is recorded by the CCD camera, which digitizes the intensity level at

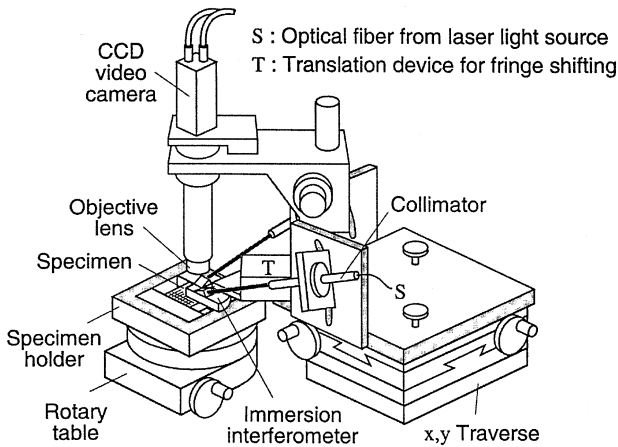


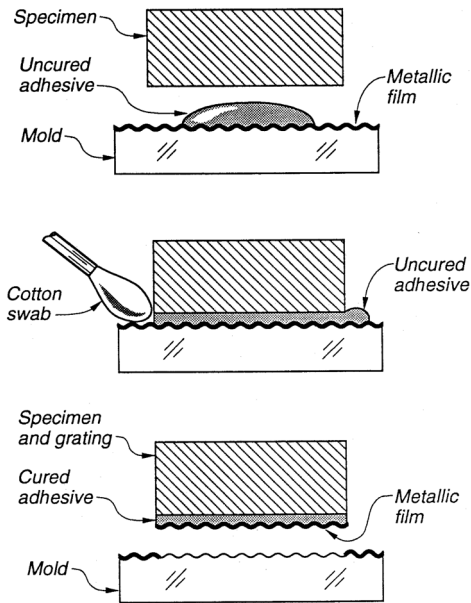
Figure 5. Mechanical and optical arrangement for microscopic moiré interferometry [2, 31].

every pixel. A piezoelectric translation device provides the means for phase stepping. The entire system is moved relative to the specimen by the  $xy$  traverse, allowing any part of the specimen to be viewed and analyzed.

### Specimen Gratings

The bar-and-space gratings of geometrical moiré cannot be printed with very high frequencies. Instead, phase gratings are used, which means that the grating surface consists of a regular array of hills and valleys. For most analyses, the specimen grating is applied by the replication process illustrated by cross-sectional views in Figure 6 [2]. A special mold is used, which is a plate with a cross-line phase grating on its surface. The grating is overcoated with a highly reflective metallic film, usually evaporated aluminum. A small pool of liquid adhesive is poured on the mold, and the specimen is pressed into the pool to spread the adhesive into a thin film. Excess adhesive is cleaned off repeatedly as it flows out. The mold is pried off after the adhesive has hardened. The weakest interface is between the metallic film and the cross-line grating, so the film is transferred to the specimen. Thus, a thin, highly reflective cross-line grating is firmly attached to the specimen surface, such that it deforms together with the specimen surface.

The adhesive thickness is typically about  $25\ \mu\text{m}$  (0.001 in.) for larger specimens (i.e., greater than  $300\ \text{mm}^2$ ) and about  $2\ \mu\text{m}$  for small specimens. For most analyses the thickness and stiffness of the grating is negligible. Various room-temperature curing adhesives can be used, including epoxies, acrylics, urethanes, and silicone rubbers. Recent reports of success with instant cyanoacrylate cements have been circulated. Adhesives that cure by exposure to ultraviolet light have been used successfully. Special techniques have been developed for replicating specimen gratings on electronic packages in order to cope with the small size and tiny openings [1, 8], as will be detailed later in the article.



**Figure 6.** Steps in producing the specimen grating by a casting or replication process; the reflective metallic film is transferred to the specimen grating [2].

## Strain Analysis

Strains can be determined from the two displacement fields by the relationships for engineering strain

$$\varepsilon_x = \frac{\partial U}{\partial x} = \frac{1}{f} \left[ \frac{\partial N_x}{\partial x} \right] \quad \varepsilon_y = \frac{\partial V}{\partial y} = \frac{1}{f} \left[ \frac{\partial N_y}{\partial y} \right] \quad (2)$$

$$\gamma_{xy} = \frac{\partial U}{\partial y} + \frac{\partial V}{\partial x} = \frac{1}{f} \left[ \frac{\partial N_x}{\partial y} + \frac{\partial N_y}{\partial x} \right] \quad (3)$$

where  $\varepsilon$  is the normal strain and  $\gamma$  is the shear strain at the surface of the specimen. Although it is not indicated here by the  $(x, y)$  suffix (shown in Eq. (1)), these equations apply for every point in the field. Thus, it is the fringe gradients that determine the strains, both the normal strains and the shear strains.

## Applications

**Grating replication for complex geometry.** A special technique is required for replicating a specimen grating on the cross sections of microelectronics devices because they usually have such a tiny and complex geometry that the excess epoxy produced by the grating replication procedure shown in Figure 6 cannot be swabbed away. The excess epoxy is critical since it could reinforce the specimen and change the local strain distribution.

An effective replication technique was developed to circumvent the problem [1, 8]. First, a tiny amount of liquid epoxy is dropped onto the grating mold; the viscosity of the epoxy should be extremely low at the replication temperature. Then, a lintless optical tissue (a lens tissue) is dragged over the surface of the mold, as illustrated in Figure 7. The tissue spreads the epoxy to produce a very thin layer of epoxy on the mold. The specimen is pressed gently into the epoxy, and it is pried off after the epoxy has polymerized. Before polymerization, the surface tension of the epoxy pulls the excess epoxy away from the edges of the specimen. The result is a specimen grating with a very clean edge. The specimen must be made very flat and smooth to be compatible with the thin film of epoxy.

**Bithermal loading.** Thermal deformations can be analyzed by room-temperature observations. In this technique, the specimen grating is applied at an elevated temperature, and it is allowed to cool to room temperature before it is observed in the moiré interferometer. Thus, the deformation incurred by the temperature increment is locked into the grating and recorded at room temperature [2, 34]. The technique is called *bithermal loading*, implying two discrete temperatures.

A typical temperature increment is  $80^{\circ}\text{C}$ , whereby the grating is applied at about  $100^{\circ}\text{C}$  and observed at about  $20^{\circ}\text{C}$ . An adhesive that cures at an elevated temperature is used, usually an epoxy. The specimen and mold are preheated to the application temperature, the adhesive is applied, and it is allowed to cure at the elevated temperature. The mold is a grating on a zero expansion substrate, so its

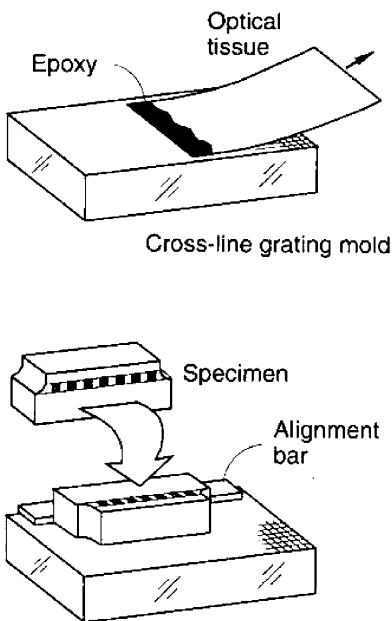


Figure 7. Procedure to replicate a specimen grating on a specimen with a complex geometry [1, 8].

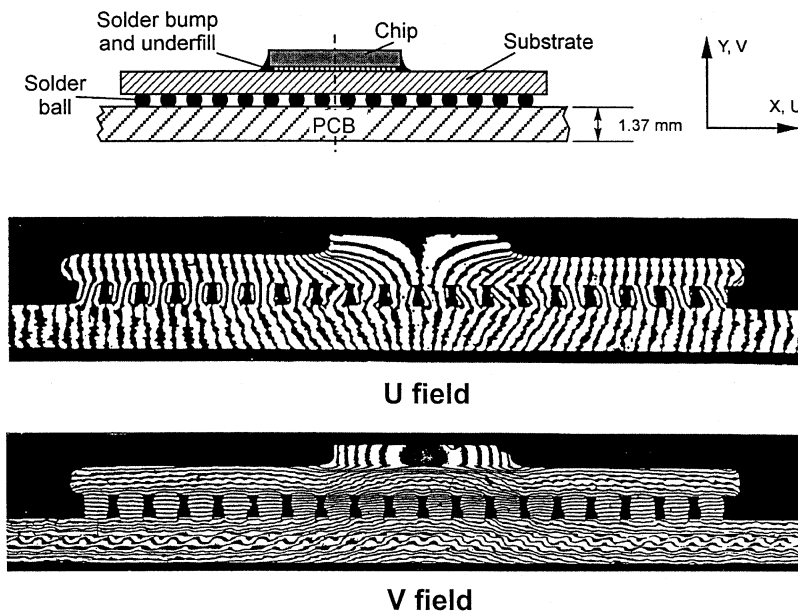


frequency is the same at elevated and room temperatures; otherwise, a correction is required for the thermal expansion of the mold.

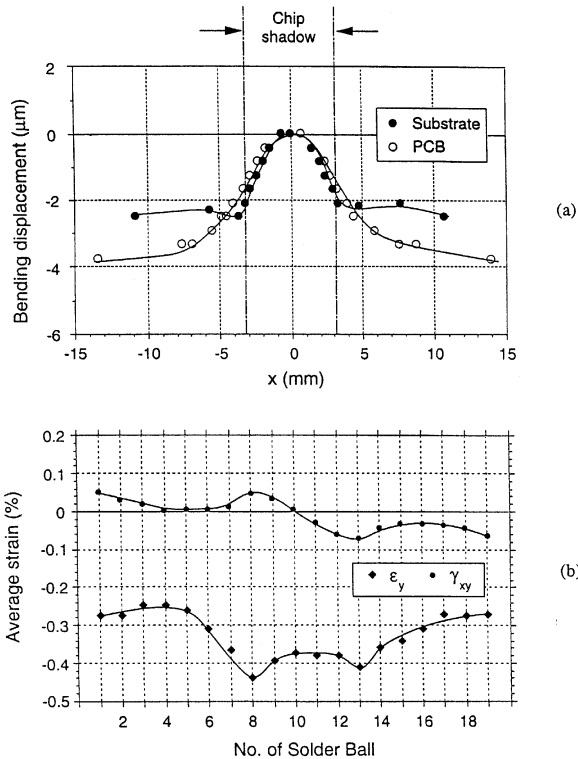
These measurements can be achieved for cryogenic temperatures, too. In one test, the specimen grating was applied at  $-40^{\circ}\text{C}$  using an adhesive that cured in ultraviolet light [2].

**Bithermal loading: Flip-chip plastic ball grid array package assembly.** An example of bithermal loading is illustrated in Figure 8 [14, 35]. The specimen is a flip-chip plastic ball grid array (FC-PBGA) package assembly. In the assembly, a silicon chip ( $6.8\text{ mm} \times 6.1\text{ mm} \times 1.2\text{ mm}$ ) was first attached to an organic substrate through tiny solder bumps. The gap between the chip and the substrate was filled with an epoxy underfill to help resist the thermal stresses induced in the solder bumps. This sub-assembly was then surface-mounted to a typical FR-4 PCB through larger solder ball arrays to form a final assembly. The assembly was cut, and its cross section was ground to produce a flat, smooth, cross-sectional surface. The specimen grating was replicated at  $82^{\circ}\text{C}$  and the fringes were recorded at room temperature ( $\Delta T = -60^{\circ}\text{C}$ ). Very clean edges of the specimen grating are evident.

The  $V$  field fringe pattern reveals the detailed bending deformation of the substrate. The vertical displacements along the centerlines of the substrate and the PCB were determined from the fringe patterns and are plotted in Figure 9a. Two distinct curvatures are observed, one in the area connected to the chip and the other in the rest of the substrate. The CTE of the substrate was higher than that of the PCB. The



**Figure 8.**  $U$  and  $V$  displacement fields of a FC-PBGA package assembly induced by thermal loading of  $\Delta T = -60^{\circ}\text{C}$  [14].



**Figure 9.** (a) Vertical displacements determined along the centerlines of the substrate and the PCB and (b) distribution of normal and shear strains (averaged along the vertical centerline) at each solder ball [35].

substrate contracted more than the PCB during cooling, while the deformation of the substrate covered by the chip was constrained by the low CTE of the chip. This complicated loading condition produced an uneven curvature of the substrate, which resulted in an inflection point below the edge of the chip.

The substrate was connected to the PCB through the solder balls, and the difference of curvature between the substrate and the PCB was accommodated by the deformation of the solder balls. The normal and shear strains (averaged along the vertical centerline) at each solder ball were calculated from the fringe patterns and are plotted in Figure 9b. The largest of these normal strains occurred in the solder ball located at the edge of the chip and its magnitude was nearly four times greater than the largest shear strain. Although symmetry about the central solder ball would be expected, the small deviations from precise symmetry are characteristic of real structures.

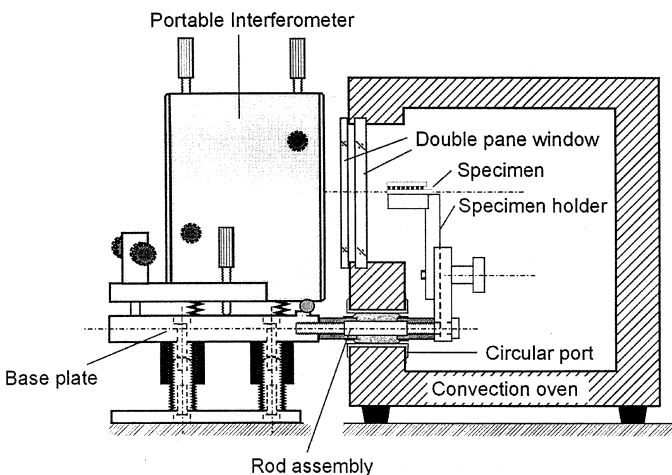
**Real-time observation: Deformation as a function of temperature.** Thermal stresses in microelectronics devices are one of the major causes of early product failure. Ideally, one would like to monitor the deformations under actual operating conditions when reliability assessment is sought. However, this is not practical because of the relatively long life cycle. The microelectronics industry has been employing accelerated

testing methods to cope with this problem, where the electronic devices are tested in much more severe environments and the results are used to predict the number of cycles to failure at the actual operating conditions by employing an acceleration parameter.

The most widely used test for reliability assessment is called the *Accelerated Thermal Cycling* (ATC) test. In the ATC test, the whole assembly is subjected to heating and cooling cycles in an environmental chamber. The electrical resistance of interconnections is monitored during thermal cycling to detect fatigue failure.

When deformation measurements are required during accelerated thermal cycling, it is necessary to implement moiré interferometry with an environmental chamber that provides convection heating and cooling. The air inside the chamber must be circulated vigorously to achieve the heating/cooling rate required for a typical ATC condition. Consequently, the environmental chamber experiences vibrations, which are normally transmitted to the specimen. Moiré interferometry measures tiny displacements, and those inadvertent vibrations can cause the moiré fringes to dance at the vibration frequency.

However, vibrations can be tolerated if there is no relative motion, that is, if the specimen and the optical system vibrate in unison. The real-time moiré setup developed to cope with the vibrations is illustrated in Figure 10 [36]. The two major components are a portable moiré interferometer (PEMI II, Photomechanics, Inc.) and a computer-controlled environmental chamber (EC1A, Sun Systems). The specimen holder is not attached to the chamber. Instead, it is connected directly to the interferometer and is essentially free from the environmental chamber. Furthermore, the interferometer and the chamber are mounted on separate tables, and thus the interferometer is mechanically isolated from the chamber. With this arrangement, the specimen vibrates together with the interferometer, and moiré fringes can be documented while the chamber is being operated. Further details of the rod assembly and the temperature control can be found in [36].



**Figure 10.** Schematic illustration of the moiré setup for real-time observation of thermal deformations [36].

**Temperature-dependent deformation of wire-bond plastic ball grid array package assembly.** The specimen was a central strip cut from a wire-bond plastic ball grid array (WB-PBGA) package assembly. The specimen assembly is depicted schematically in Figure 11*a* with relevant dimensions. In the package, an active chip is first bonded to the substrate, which is a thin PCB, and the integrated circuits are connected electrically to the bond fingers on the substrate by thermosonic gold wire bonding. The device is then overmolded to form a PBGA package. For the final assembly, the package is connected mechanically and electrically to a thicker PCB using a uniform array of solder balls.

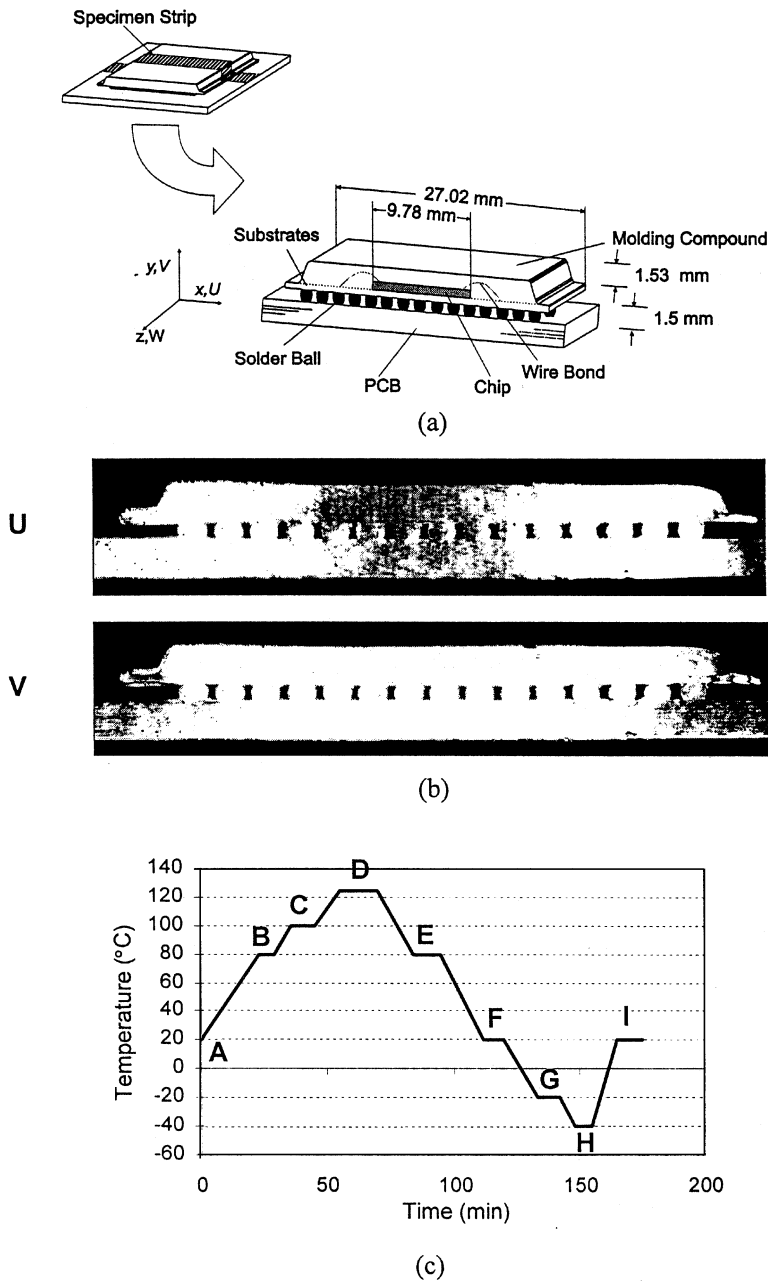
The cross section was ground flat by a 600-grit abrasive paper. The drag method [1, 8] was utilized to replicate a specimen grating using a room temperature curing epoxy (Tra-100, Tracon). The initial null fields obtained at room-temperature are shown in Figure 11*b*. The clean edges obtained by the drag method are evident.

The specimen was subjected to a thermal cycle, and the deformations were documented as a function of temperature. Figure 11*c* depicts the temperature profile used in the thermal cycle. The maximum and minimum temperatures were 125°C and -40°C, respectively.

Representative fringe patterns obtained at 80°C (heating), 125°C, 80°C (cooling), and -20°C are shown in Figure 12. The thermal deformation in the assembly is very complicated. The magnitude and the direction of the deformation depend on the temperature-dependent thermal/mechanical properties of materials used in the assembly. The vertical or bending displacements along the centerline of the package (along the line A-B in the insert of Figure 13) were determined from the fringe patterns, and the results are plotted in Figure 13 to illustrate the complexity.

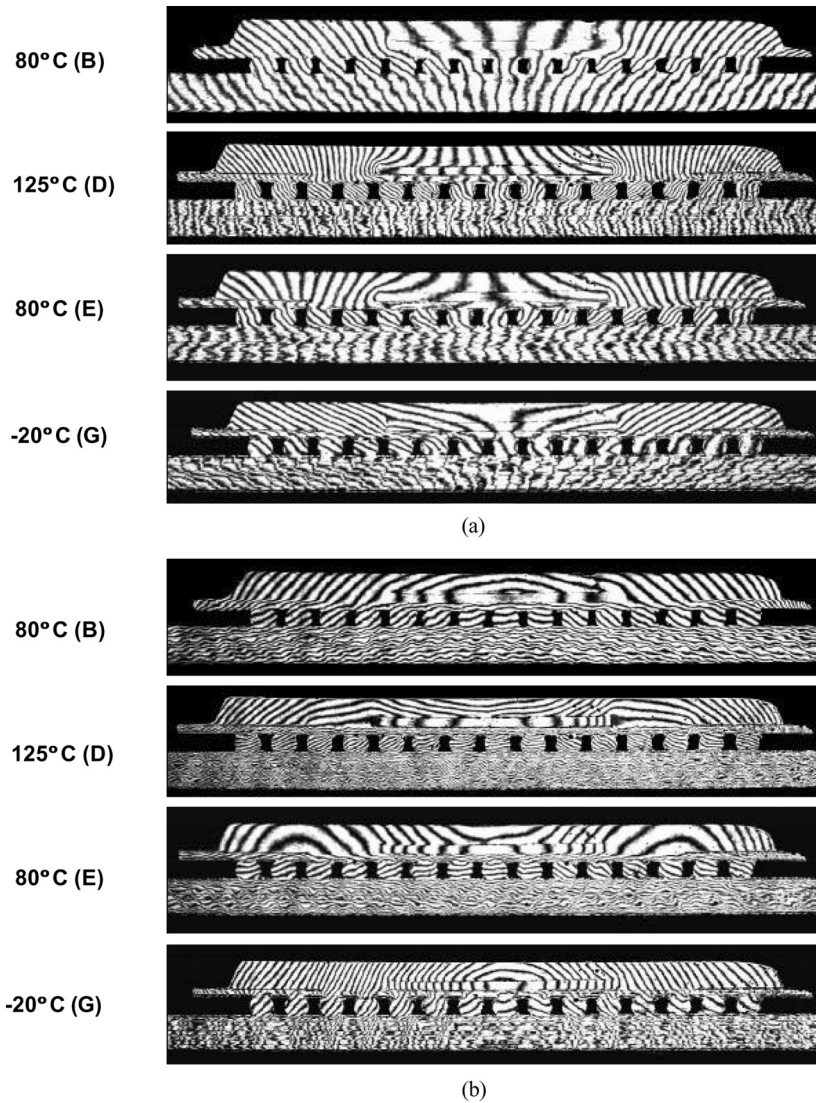
Before the solder material relaxes at a high temperature, the coupling between the package and the PCB through the solder balls dominates. The effective CTE of the package ( $\approx 10$  ppm/°C) is much lower than that of the PCB and thus the package bent upward ( $\cup$ ) at the initial heating stage; the PCB expands more than the package. When the stress in the solder balls relaxes at a high temperature because of creep deformation, the coupling between the package and the PCB is reduced and the deformation of the package is governed by the constraints within the package.

As can be seen from Figure 13, the bending displacement of the part of the package containing the chip assumes an opposite position ( $\cap$ ) at 125°C compared to that at 80°C. The change is ascribed to the coupling between the molding compound (CTE = 16 ppm/°C) and the chip (CTE = 3 ppm/°C). The molding compound expands more than the chip, and that part of the package bent downward after the coupling between the package and the PCB diminished. However, the bending direction of the rest of the package did not change at 125°C because the effect of the chip did not exist in this area. It is important to note that the stress relaxation at 125°C changed the reference point of zero stress in the solder. As a result, the deformation of the package at 80°C (cooling) was influenced by the deformed configuration at 125°C, and thus it was significantly different from the deformation at 80°C (heating). Such experimental data is critical when verifying a numerical model for a parametric study for design optimization.



**Figure 11.** (a) Schematic diagram of specimen geometry with relevant dimensions, (b) initial null fields obtained at room temperature, and (c) temperature profile used in the experiment [36].

**Accumulated plastic deformation in solder interconnection.** The assembly used in the experiment was a 25-mm CBGA package assembly with 361 I/O's (19 × 19 solder



**Figure 12.** Representative (a)  $U$  field and (b)  $V$  field fringe patterns [36].

interconnection array) assembled to an FR-4 PCB. A specimen with a strip array configuration was prepared from the assembly, containing five central rows of solder interconnection. The solder interconnection of the package assembly consists of a high-melting-point solder ball (90%Pb/10%Sn) and a eutectic solder fillet (63%Pb/37%Sn). The high-melting-point solder ball does not reflow during the assembly process, which provides a consistent and reproducible standoff between the ceramic package and the PCB (see Figure 3).

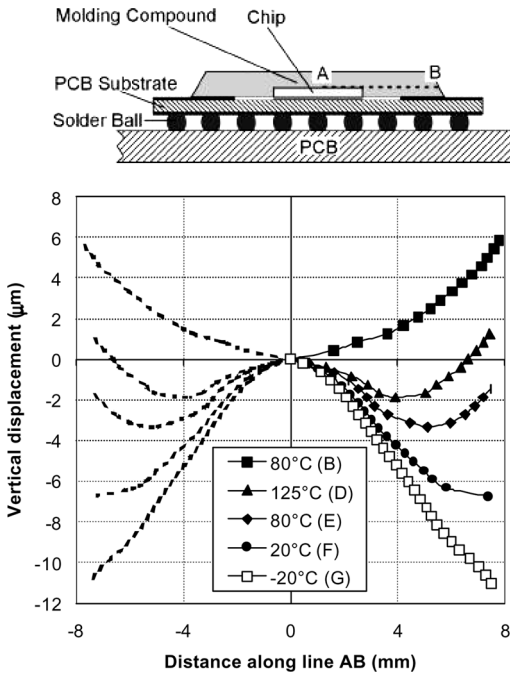


Figure 13. Bending displacements obtained along the line shown in the insert [36].

The diameter of the solder ball was 0.89 mm. After the interconnection was formed, the actual separation from the package to the PCB was 0.97 mm. The pitch of the copper pads on the PCB was 1.27 mm. The specimen was subjected to a thermal cycle, and the deformations were documented as a function of temperature.

The dominant mode of deformation of the solder interconnection is shear deformation, which is caused by the mismatch of the CTE of the ceramic module and the PCB. Consequently, the shear strains at the interconnection increase as the DNP increases. The development of inelastic strains during the thermal cycle is explained in Figure 14, where the fringe patterns for the rightmost solder interconnection are shown. The corresponding horizontal displacements along the vertical centerlines are plotted for various stages in the thermal cycle.

As the temperature increased, a relative horizontal displacement between the top and the bottom of the solder interconnection was caused by the CTE mismatch between the module and the PCB. The relative displacement was virtually linear over the height of the solder interconnection at the initial stage of heating (B), which indicated a nearly uniform shear strain in the interconnection. As the temperature increased, however, the slope at the high-melting solder ball became distinctively different from that at the eutectic solder fillet. At the elevated temperatures, the shear strain of the eutectic fillet became much larger than that of the solder ball. The eutectic fillet has a much lower melting point compared to the solder ball, and thus it has a smaller modulus and a higher creep rate at elevated temperatures. As a result,

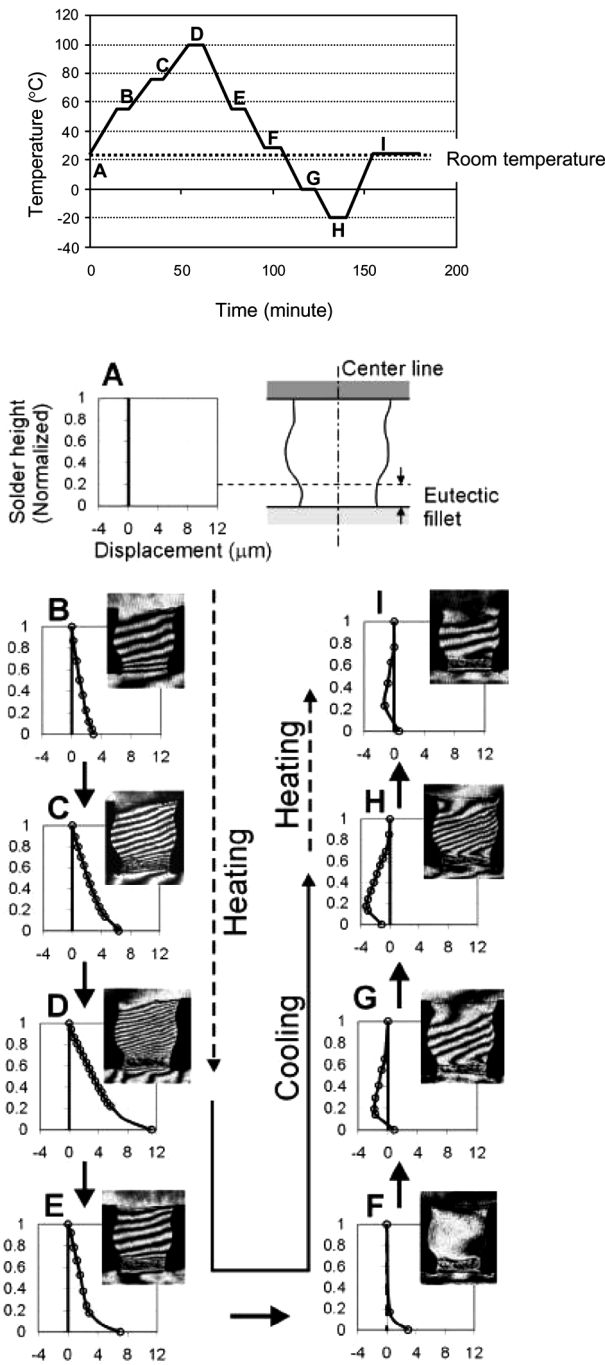


Figure 14. *U* field fringe patterns of the rightmost solder interconnection of CBGA package assembly and the corresponding horizontal displacements determined along the vertical centerline [37].



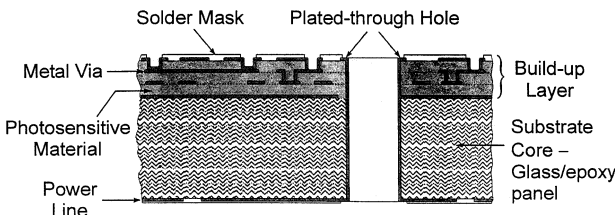
the shear strain of the eutectic fillet increased at a much higher rate than that of the solder ball.

The most striking results were observed during cooling. When the assembly was cooled to 55°C (E) from the maximum temperature, the relative horizontal displacement (or average shear strain) of the high-melting-temperature solder ball was identical to the deformation observed at the same temperature during heating (B). However, the shear strain in the eutectic fillet below the ball was much higher because the creep strain produced at the maximum temperature was not recovered during cooling. When the assembly was cooled down to room temperature, this became more evident. The shear strain in the ball recovered completely, but the shear strain in the fillet did not. As the assembly was cooled to cryogenic temperatures, the solder ball exhibited the opposite relative horizontal displacement as expected but the direction of the relative horizontal displacement in the eutectic fillet remained unchanged. As a result, the sign of the shear strain of the solder ball became opposite to that of the eutectic fillet.

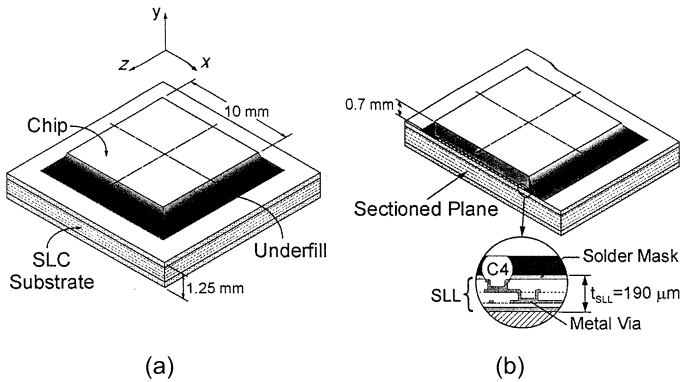
The shear strain in the eutectic fillet increased rapidly at high temperatures. Its maximum value was  $\approx -2.4\%$  at 100°C, which was nearly six times as large as the shear strain in the solder ball. While the assembly was cooled to room temperature (F), the shear strain magnitude decreased at a much slower rate. The permanent shear strain in the eutectic fillet was  $\approx -1.5\%$  after the heating cycle.

**Micromechanics: Micro via in built-up structure.** One of several purposes of a chip carrier is to provide conducting paths between the extremely compact circuits on the chip and the more widely spaced terminals on the PCB. Recent micro via technology enabled the industry to produce laminate substrates with high density and fine pitch conductors as required for advanced assemblies. A cross-sectional view of a high-density organic substrate is illustrated in Figure 15 [38]. Photosensitive dielectric layers (insulators) are built up sequentially with patterned layers of copper plating (typically 25  $\mu\text{m}$  thick).

Extensive research and development efforts have been and are being made to perfect the underfill process for these organic substrates and to develop optimum underfill materials for the larger silicon devices. An important trend in newly developed underfill materials is its increased Young's modulus, which increases the coupling between the silicon chip and the substrate. This high degree of coupling transfers the CTE mismatch induced-loading to the built-up layers of the substrate.



**Figure 15.** Schematic diagram of a high-density organic substrate with built-up structures [38].



**Figure 16.** Schematic diagram of the flip-chip assembly on a high-density substrate (a) before and (b) after specimen preparation [21].

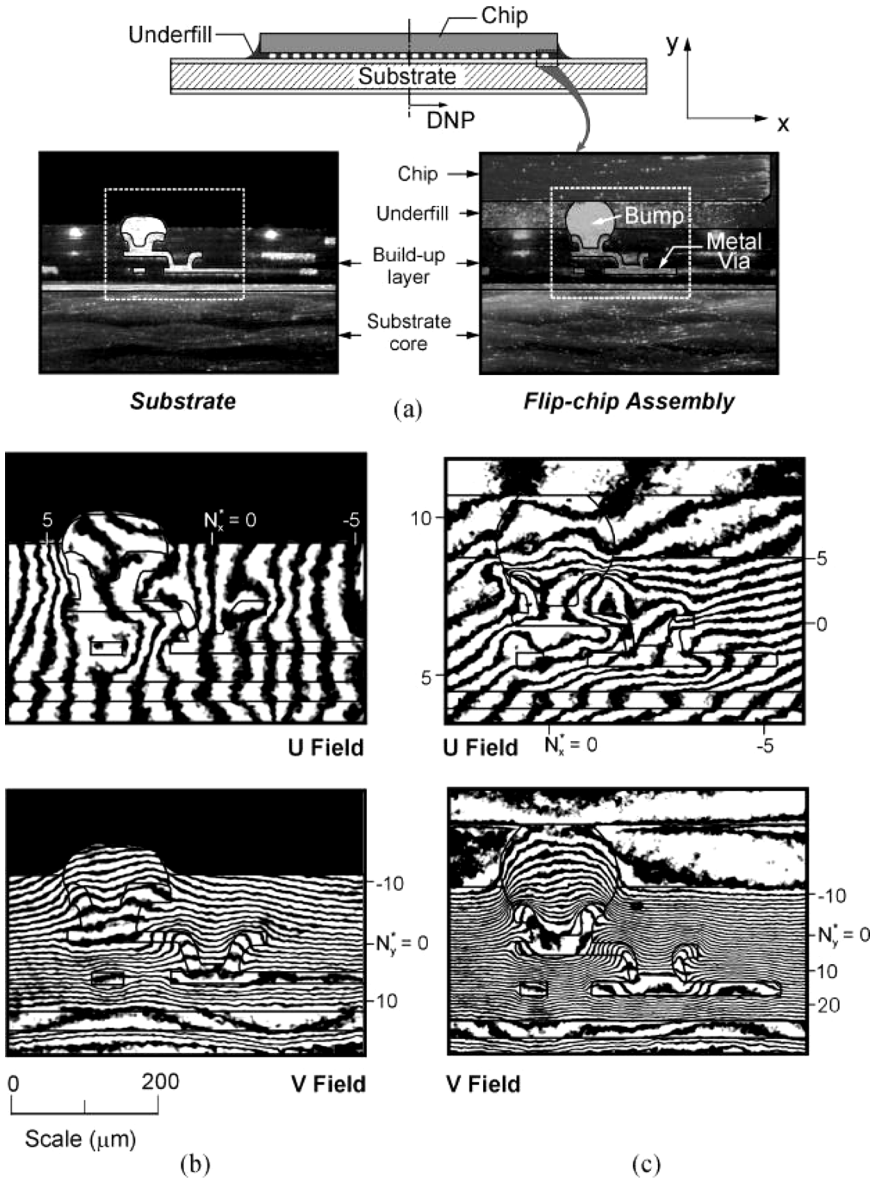
Microscopic moiré interferometry was employed to quantify the effect of the underfill on the deformations of the microstructures within the built-up layers. Two specimen configurations were analyzed to study the deformations induced by the subsequent manufacturing process: a bare substrate and a flip-chip package. The flip-chip assembly is illustrated schematically in Figure 16a with its relevant dimensions. In the assembly, a silicon chip was attached to a high-density substrate by solder bumps and the gap between the solder bumps was filled with an underfill.

The specimens were cut and ground to expose the desired microstructures as illustrated schematically in Figure 16b, where the insert depicts the detailed microstructures within the built-up layer. An epoxy specimen grating was applied at an elevated temperature of  $92^{\circ}\text{C}$  in a small region containing the microstructures. A tiny volume of the epoxy was applied around the region of interest with a sharp-pointed tool and a ULE grating mold was pressed against the epoxy to spread it into a thin film over the region. The fringes were recorded at a room temperature of  $22^{\circ}\text{C}$ , recording the thermal deformation for  $\Delta T = -70^{\circ}\text{C}$ .

The displacement fields for a small region containing the microstructures were recorded by microscopic moiré interferometry. The region is marked by a dashed box in Figure 17a; it is approximately  $500\ \mu\text{m} \times 375\ \mu\text{m}$ . The resultant fringe patterns are shown in Figure 17 for (b) the bare substrate and (c) the flip-chip assembly. A fringe multiplication factor of  $\beta = 4$  was used to produce a displacement contour interval of  $52\ \text{nm}/\text{fringe}$ .

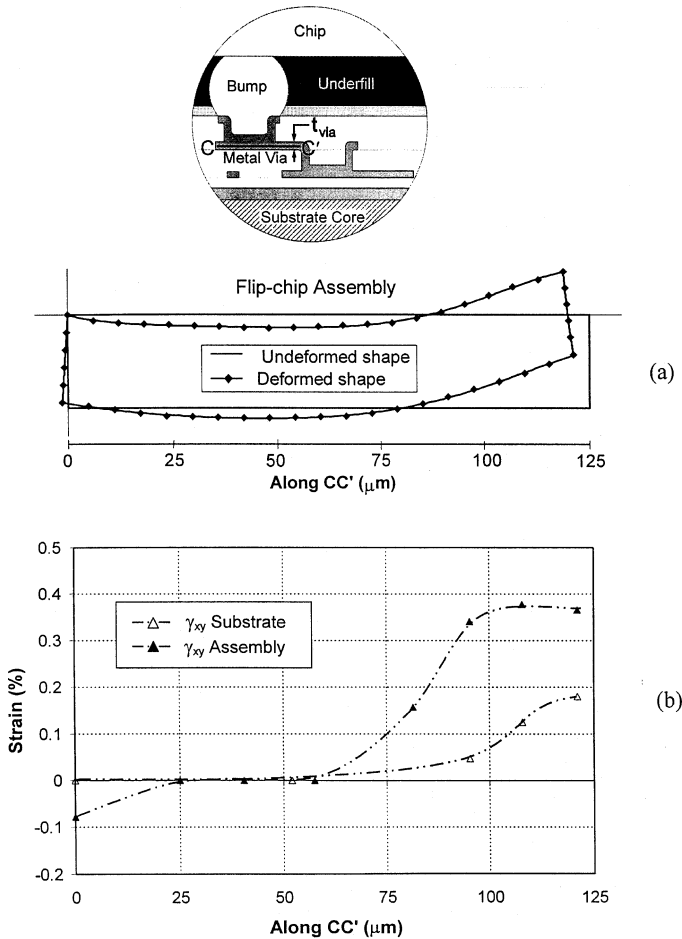
The copper micro vias are imbedded in the built-up layer. The CTE of the copper ( $17\ \text{ppm}/^{\circ}\text{C}$ ) is much smaller than the CTE of the photosensitive material ( $>40\ \text{ppm}/^{\circ}\text{C}$ ). Consequently, the photosensitive material contracts more than the via during cooling. Since the photosensitive material is confined by the metal via and the adjacent layer, the different expansion rate causes deformations within the metal vias.

The deformation of a small segment of metal via,  $CC'$  (see the insert of Figure 18), was analyzed to investigate the effect of the chip and underfill. The deformed shape of the portion  $CC'$  in the flip-chip assembly was evaluated from the fringe patterns in Figure 17c and the results are plotted in Figure 18a.



**Figure 17.** (a) Micrographs of the region of interest. Microscopic  $U$  and  $V$  displacement fields of (b) bare substrate and (c) flip-chip assembly. The contour interval is 52 nm per fringe [21].

The center portion of  $CC'$  is connected rigidly to the solder bump/underfill layer while the left and right segments are extended into the photosensitive material. As can be seen from the deformed shape, these segments moved in the positive  $y$ -direction (upward) relative to the center portion. This movement produced a shear



**Figure 18.** (a) Deformed shape of the micro via segment  $CC'$  in the flip-chip assembly and (b) shear strain distribution along  $CC'$  [21].

strain in the segments, which is plotted in Figure 18b. The maximum shear strain occurred near the end of the right segment, and its magnitude was 0.38%. The shear strain of the same segment in the bare substrate is also plotted in Figure 18b. The effect of the extra constraint from the solder and underfill layer is evident.

## THERMAL WARPAGE ANALYSIS

### Twyman/Green Interferometry

**Basic principle.** Twyman/Green (T/G) interferometry is an optical method, which measures surface contours (out-of-plane displacements) with submicron sensitivity [2]. T/G interferometry is simple, but it can be used very effectively to

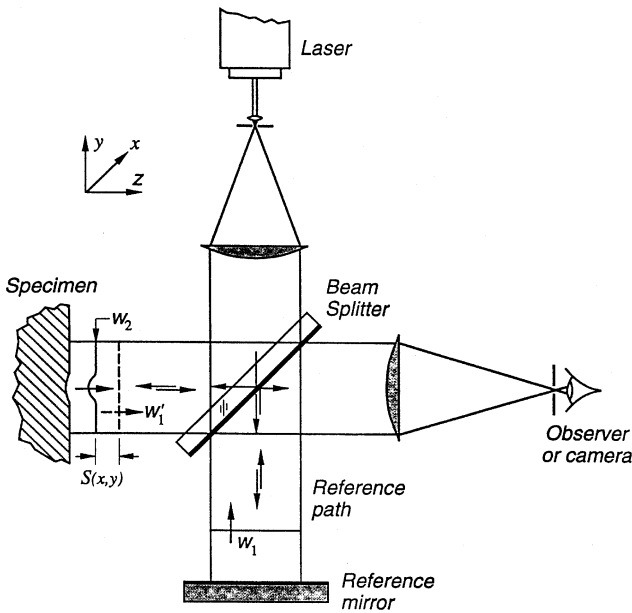


Figure 19. Schematic diagram of T/G interferometry [2].

determine deflections of silicon wafers or chips. The silicon surface is polished during the manufacturing process and provides a specular (mirror-like) surface, which is a critical requirement for the method. More importantly, the method can be used together with moiré interferometry to provide a complete set of  $U$ ,  $V$ ,  $W$  displacement fields since the moiré specimen grating also provides the required specular surface on the specimen.

Figure 19 illustrates the optical setup schematically. In the method, an optically flat beam splitter directs half the light to the specimen and the other half to a flat reference mirror. After reflection from the specimen and reference surfaces, the beams meet again at the beam splitter and a portion of each propagates horizontally to be collected by an imaging system. The wavefront from the specimen ( $W_2$ ), which was originally flat, interferes with the wavefront from the reference mirror ( $W_1$ ) to produce a contour map of the  $z$ -coordinate of the specimen surface. The  $W$  displacement then can be determined by

$$W(x, y) = \frac{\lambda}{2} N_z(x, y) \quad (4)$$

where  $N_z$  is the fringe order at each point in the fringe pattern and  $\lambda$  is the wavelength of the laser light employed. When an He-Ne laser of  $\lambda = 0.633 \mu\text{m}$  is used, the contour interval of the fringe pattern is  $0.316 \mu\text{m}$  per fringe order.

**Application: Tape automated bonding assembly.** The package studied by T/G interferometry was a typical chip/heat sink assembly. The package used the tape

automated bonding (TAB) technology, where a small active chip (5 mm square for this case) was joined to patterned metal on polymer tape using thermocompression bonding. Then, the top surface of the chip was protected by dispensing an encapsulant. The chip/tape subassembly was later adhesively bonded to an aluminum heat sink to form a final package.

When the subassembly cooled to room temperature after the encapsulant was cured at an elevated temperature, the encapsulant bent the chip, as illustrated schematically in Figure 20 [12]. The bending was caused by thermal contraction of the encapsulant, which created a large tensile stress on the chip/heat sink adhesive layer. This bending had to be portrayed accurately, since excess tensile stresses caused by the chip bending could produce cracks in the adhesive layer.

The results from the subassemblies with different thicknesses of encapsulant are shown in Figure 20. The fringe patterns represent the bending deformation of the back side of the chip at room temperature. The corresponding bending displacement was determined from Eq. (4). The results indicated that the bending displacement was linearly proportional to the amount of encapsulant. With a given chip and heat sink material, the tensile stresses of the adhesive layer increased as the amount of

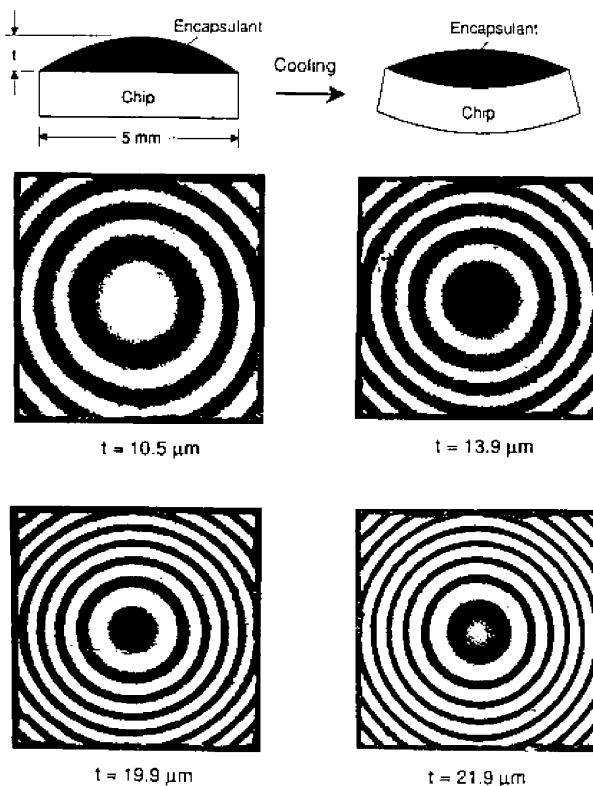


Figure 20. Surface contours of silicon chip caused by thermal contraction of the encapsulant [12].

the encapsulant (and the subsequent bending) increased. The results were used to provide a manufacturing specification of the allowable maximum encapsulation thickness.

### Shadow Moiré

**Basic principle.** Shadow moiré provides whole-field maps of out-of-plane displacements but with relatively coarse sensitivity (typically 25 to 50  $\mu\text{m}$  per fringe order). The method does not require any special surface condition. The sensitivity range and relaxed surface requirement make the method ideally suited for the warpage measurement of PCB and chip/organic carrier packages [24–28].

In the method, a real reference grating is located in front of a specimen and it creates moiré fringes by interrogating with its shadow on the specimen. Figure 21 illustrates the basic concepts of real-time shadow moiré [16]. A linear reference grating of pitch  $g$  is fixed adjacent to the surface, which serves as a window of an environmental chamber. The grating is comprised of black bars and clear spaces on a flat glass plate. A light source illuminates the grating and specimen, and the observer (or camera) receives the light that is scattered in its direction by the matte specimen.

With the arrangement shown in Figure 21, where the source and camera lie at the same distance from the plane of the specimen, the relationship between  $W$  and fringe order  $N_z$  is

$$W(x, y) = \frac{g}{\tan \alpha + \tan \beta} N_z(x, y) = \frac{gL}{D} N_z(x, y) \quad (5)$$

where  $W$  and  $N_z$  apply to each  $x, y$  point in the field. Although incidence and viewing angles  $\alpha$  and  $\beta$ , respectively, vary across the field, the sum of their tangents is a constant.

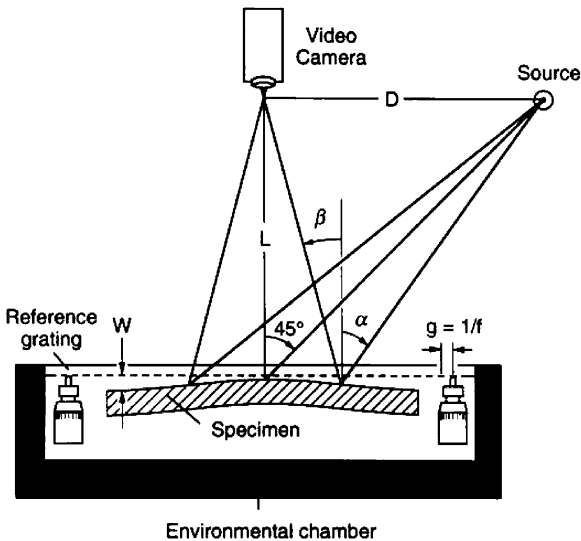


Figure 21. Schematic diagram of real-time shadow moiré setup [16].

In practice, the sensitivity of shadow moiré is limited by the undesired diffraction effect of a reference grating, which decreases fringe visibility or contrast. A reference grating of 20 lines/mm (500 lines/in.) was often used as a practical upper limit.

**Popcorn effect in wire bond plastic ball grid array package.** The WB-PBGA package is not a hermetically sealed package, and thus the plastic mold compound (PMC) absorbs moisture while the package is in storage. The absorbed moisture is usually condensed at the chip/substrate interface. When the package is heated rapidly in a reflow oven, the moisture vaporizes and produces a high pressure, which cracks the package; this phenomenon is known as the *popcorn effect* [39]. Real-time shadow moiré was employed to document the effect.

The specimen was a 35-mm square WB-PBGA package. The results obtained from shadow moiré are shown in Figure 22, which represent the warpage of the substrate (bottom) side of the package with a contour interval of 50  $\mu\text{m}$  (2 mil) per fringe. The out-of-plane displacements along a diagonal line were extracted from the fringe patterns, and the results are plotted in Figure 22. At 200°C, a highly concentrated warpage occurred over the chip area. The total warpage over the area was 100  $\mu\text{m}$ , and it was ascribed to initial vapor expansion that delaminated the interface between the chip and chip pad. As the temperature increased, the pressure developed by the vapor increased. As a result, delamination eventually propagated through the PMC/substrate interface at 240°C, indicated by the uniformly distributed circular fringes in the pattern.

## Far Infrared Fizeau Interferometry

**Basic principle.** Although simple, the application of T/G interferometry is limited since it requires a specular (mirror-like) surface. In addition, its measurement sensitivity is a fraction of a micron, which is usually too high for typical warpage observed in the flip-chip packages. On the other hand, with shadow moiré, a small distance between the specimen and the reference grating is required for fringe formation; consequently, the chip and the substrate cannot be viewed simultaneously. In addition, a diffusive surface is required for good fringe visibility, which is typically accomplished by spraying a white matte paint and is not desired for nondestructive testing.

For the FC-PBGA package applications, the measurement sensitivity in the range of microns is ideal. Large tolerance in specimen surface roughness is required to test the ground surface of the chip and the organic substrate without any specimen preparation. The warpage is to be measured as a function of temperature to simulate operating and accelerated testing conditions. These technical requirements were the immediate motivation of development of far infrared Fizeau interferometry (FIFI).

It has been known that the specular component of the reflected light (mirror-like reflection) increases as the wavelength or the angle of incidence increases. Consequently, with a longer wavelength, a surface regarded as optically rough under visible light can be treated as a specular surface. The increase of specular reflection can be explained qualitatively using the definition of effective roughness,  $\varepsilon_R$ , known as the “Rayleigh criterion”



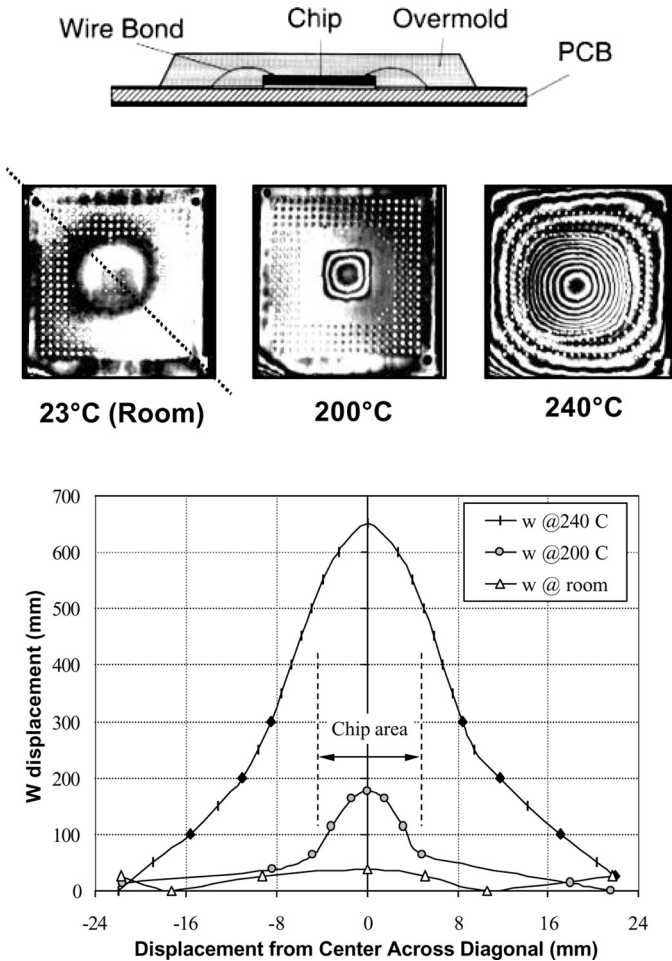


Figure 22. Warpage of WB-PBGA package caused by popcorn effect, where a contour interval is 50 μm per fringe order.

$$\epsilon_R = \frac{4\pi h \cos \theta}{\lambda} \tag{5}$$

where  $h$  is height of the surface irregularities,  $\lambda$  is the wavelength, and  $\theta$  is the angle of incidence. Theoretically, a surface will become perfectly smooth when  $h/\lambda$  approaches zero or  $\theta$  approaches  $90^\circ$ .

Fizeau interferometry is a classical interferometry using visible light, which measures surface topography of a slightly warped specular surface. Far infrared Fizeau interferometry extends the domain of its application by employing light with

a very long wavelength, thus decreasing the effective roughness of the specimen surface [40]. Considering  $\lambda = 10.6 \mu\text{m}$  of the  $\text{CO}_2$  laser, the effective roughness is reduced by a factor of 20 for a given angle of incidence, compared with a wavelength in the middle of the visible spectrum (green light with  $0.5 \mu\text{m}$ ). Consequently, optically rough surfaces such as the ground surface of silicon and organic substrate can be tested without any specimen preparation.

The optical configuration of FIFI is explained in Figure 23a [29]. The beam from the laser is first divided by a partial reflector to reduce the intensity of the laser. The transmitted light is expanded and is subsequently collimated by a collimating lens. An optical flat is placed next to the collimating lens. The optical axis of the collimating lens is perpendicular to the optical flat, and the expanded beam illuminates them with a small angle of incidence. A portion of the collimated beam is reflected from the optical flat, while the transmitted beam is reflected from the specimen surface. The reflected beams are collected by an infrared CCD camera.

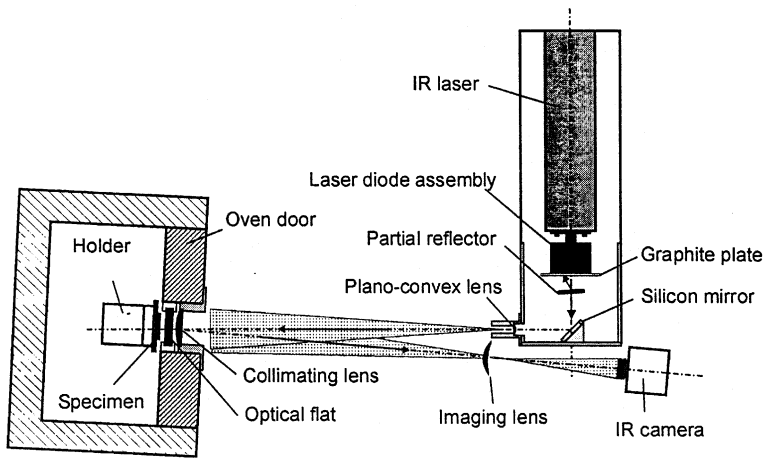
The wavefront from the optical flat, which is originally flat, interferes with the wavefront from the specimen to produce a contour map of the  $z$ -coordinate of the surface. The  $W$  displacement can then be determined by

$$W(x, y) = \frac{\lambda}{2 \cos \theta} N_z(x, y) \quad (6)$$

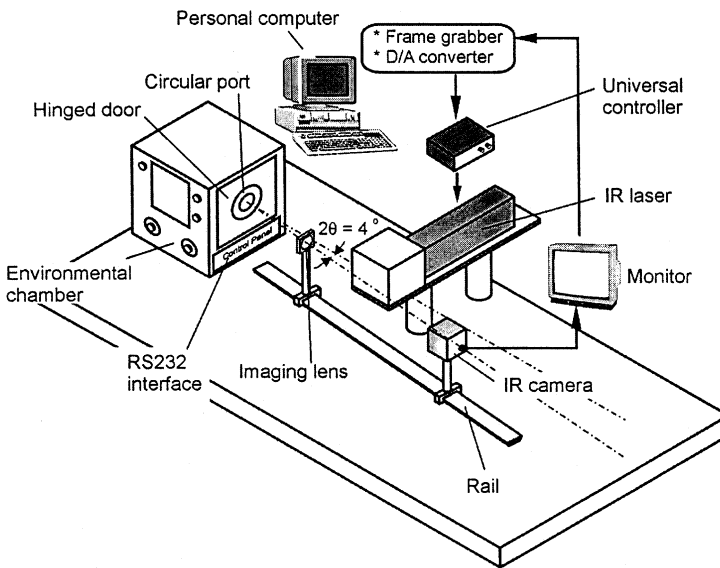
where  $N$  is the fringe order at each point in the fringe pattern,  $\theta$  is an angle of incidence, and  $\lambda$  is the wavelength of the laser light employed. With a small angle used in the system ( $\cos \theta \approx 1$ ), the measurement sensitivity is defined as  $\lambda/2$  per fringe order ( $5.3 \mu\text{m}$  per fringe order).

The mechanical configuration for real-time observation is illustrated in Figure 23b [29]. An air-cooled  $\text{CO}_2$  laser is used as a coherent light source. An expanded beam illuminates the optical flat and the collimator mounted on a specially designed port of an environmental chamber. The imaging system is comprised of an imaging lens and an infrared CCD camera. The imaging lens is mounted on a translation stage that travels along a rail to provide a desired magnification factor for various sizes of specimens. The image is displayed on a monitor, and the output from the monitor is digitized by a frame grabber for image processing.

**Characterization of FC-PBGA package behavior.** Warpage behavior of an FC-PBGA package was evaluated by FIFI [41]. The cross-sectional view of the package is shown in Figure 24. A square chip ( $12 \text{ mm} \times 12 \text{ mm}$ ) was mounted on a BT-based substrate ( $31 \text{ mm} \times 31 \text{ mm}$ ). Initially, the package was heated to an underfill curing temperature ( $150^\circ\text{C}$ ). Then, the deformations of the top surface of the package were documented while cooling the package to room temperature. The fringe patterns obtained at  $150^\circ\text{C}$ ,  $100^\circ\text{C}$ , and room temperature are shown in Figure 24a–c, where the contour interval is  $5.3 \mu\text{m}$  per fringe order. The package was virtually flat (devoid of fringes) at the underfill curing temperature.



(a)

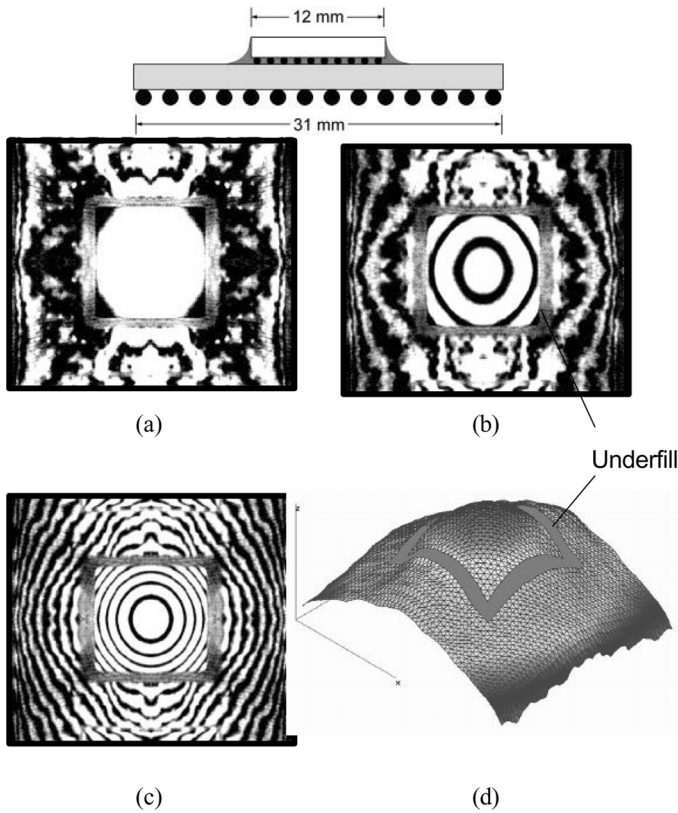


(b)

**Figure 23.** (a) Optical and (b) mechanical configuration of FIFI for real-time observation [29].

The large mismatch in CTE caused the package to bend as the temperature decreased.

It is important to note that the fringe patterns from the chip and the substrate were recorded from a single experiment, although the surfaces of the silicon



**Figure 24.** Warpage contours of FC-PBGA package documented at (a) 150°C, (b) 100°C, and (c) room temperature, where the contour interval is 5.3  $\mu\text{m}$  per fringe order. (d) A three-dimensional warpage map at room temperature obtained by digital image processing [41].

and the substrate were not located in the same plane. In addition, the high signal-to-noise ratio provided by the fringes on the rough surfaces of the chip and the substrate clearly indicates the highly effective roughness tolerance of the method.

A three-dimensional representation of the warpage at room temperature is shown in Figure 24d, which reveals a significant bending in both chip and substrate. Irregularities shown in the substrate are not caused by optical noise. Instead, they represent the heterogeneous deformation of the multi-ply glass/epoxy composite.

With the flip-chip technology, the conventional orientation of the chip is reversed. The chip is placed face down, and the connection between the chip and the chip carrier is achieved by solder bumps. Because of this new orientation, the top surface of the chip is available for enhanced thermal management solutions. However, the inherently large warpage of FC-PBGA packages poses a new technical challenge in the high-performance thermal solution, that is, nonuniform thermal conductance at the chip/heat sink interface [41, 42]. The results from FIFI can be used to assess the performance of thermal interfaces with non-adhesive-type interstitial materials.

## SUMMARY

Several photomechanics methods were presented for thermal stress analyses of microelectronics devices. Recent developments and features of the methods were reviewed and selected applications were illustrated. The in-situ and quantitative nature of the methods led to more accurate and realistic understanding of the macro- and micro-thermomechanical behavior of microelectronics assemblies and interconnections, which in turn facilitated design evaluation and optimization at an early stage of product development. The whole-field information with various sensitivities and resolutions provided by the methods made them ideally suited for the deformation study of a broad range of problems in microelectronics packaging. A more extensive range of applications is anticipated.

## REFERENCES

1. B. Han, Recent Advancement of Moiré and Microscopic Moiré Interferometry for Thermal Deformation Analyses of Microelectronics Devices, *Exper. Mech.*, vol. 38, no. 4, pp. 278–288, 1998.
2. D. Post, B. Han, and P. Ifju, *High Sensitivity Moiré: Experimental Analysis for Mechanics and Materials*, Springer-Verlag, New York, 1994. Also D. Post, B. Han, and P. Ifju, Moiré Methods for Engineering and Science—Moiré Interferometry and Shadow Moiré, in Pramod Rastogi (ed.), *Photomechanics for Engineers*, Ch. 7, Springer-Verlag, New York, 2000.
3. G. Cloud, *Optical Methods of Engineering Analysis*, Cambridge Univ. Press, New York, 1995.
4. A. F. Bastawros and A. S. Voloshin, Transient Thermal Strain Measurements in Electronic Packages, *IEEE Trans. Components, Hybrids and Manufacturing Tech.*, vol. 13, no. 4, pp. 961–966, 1990.
5. A. F. Bastawros and A. S. Voloshin, In Situ Calibration of Stress Chips, *IEEE Trans. Components, Hybrids and Manufacturing Tech.*, vol. 13, no. 4, pp. 888–892, 1990.
6. A. F. Bastawros and A. S. Voloshin, Thermal Strain Measurements in Electronic Packages through Fractional Fringe Moiré Interferometry, *J. Elec. Packaging, Trans. ASME*, vol. 112, no. 4, pp. 303–308, 1990.
7. Y. Guo, W. T. Chen, and C. K. Lim, Experimental Determination of Thermal Strains in Semiconductor Packaging Using Moiré Interferometry, *Proceedings of 1992 Joint ASME/JSME Conference on Electronic Packaging*, pp. 779–784, American Society of Mechanical Engineers, New York, 1992.
8. Y. Guo, W. T. Chen, C. K. Lim, and C. G. Woychik, Solder Ball Connect (SBC) Assemblies under Thermal Loading: I. Deformation Measurement via Moiré Interferometry, and Its Interpretation, *IBM J. Res. Dev.*, vol. 37, no. 5, pp. 635–648, 1993.
9. T. Y. Wu, Y. Guo, and W. T. Chen, Thermal-Mechanical Strain Characterization for Printed Wiring Boards, *IBM J. Res. Dev.*, vol. 37, no. 5, pp. 621–634, 1993.
10. B. Han and Y. Guo, Thermal Deformation Analysis of Various Electronic Packaging Products by Moiré and Microscopic Moiré Interferometry, *J. Elec. Packaging, Trans. ASME*, vol. 117, pp. 185–191, 1995.
11. P. H. Tsao and A. S. Voloshin, Manufacturing Stresses in the Die Due to Die-Attach Process, *IEEE Trans. Components, Packaging and Manufacturing Tech. Pt. A*, vol. 18, no. 1, pp. 201–205, 1995.
12. B. Han, Y. Guo, C. K. Lim, and D. Caletka, Verification of Numerical Models Used in Microelectronics Packaging Design by Interferometric Displacement Measurement Methods, *J. Elec. Packaging, Trans. ASME*, vol. 118, pp. 157–163, 1996.
13. B. Han and Y. Guo, Determination of Effective Coefficient of Thermal Expansion of Electronic Packaging Components: A Whole-Field Approach, *IEEE Trans. Components, Packaging and Manufacturing Tech. Pt. A*, vol. 19, no. 2, pp. 240–247, 1996.
14. B. Han, M. Chopra, S. Park, L. Li, and K. Verma, Effect of Substrate CTE on Solder Ball Reliability of Flip-Chip PBGA Package Assembly, *J. Surface Mount Tech.*, vol. 9, pp. 43–52, 1996.

15. B. Han, Deformation Mechanism of Two-Phase Solder Column Interconnections under Highly Accelerated Thermal Cycling Condition: An Experimental Study, *J. Elec. Packaging, Trans. ASME*, vol. 119, pp. 189–196, 1997.
16. B. Han and Y. Guo, Photomechanics Tools as Applied to Electronic Packaging Product Development, in B. Han, R. Mahajan, and D. Barker (eds.), *Experimental/Numerical Mechanics in Electronics Packaging*, vol. 1, pp. 11–15, Society for Experimental Mechanics, Bethel, CT, 1997.
17. J.-H. Zhao, X. Dai, and P. S. Ho, Analysis and Modeling Verification for Thermal-mechanical Deformation in Flip-Chip Packages, *Proceedings of 48th Electronic Components and Technology Conference*, pp. 336–344, May 25–28, Seattle, WA, 1998.
18. A. S. Voloshin, P. H. Tsao, and R. A. Pearson, In situ Evaluation of Residual Stresses in an Organic Die-Attach Adhesive, *J. Elec. Packaging, Trans. ASME*, vol. 120, no. 3, pp. 314–318, 1998.
19. B. Han, Z. Wu, and S. Cho, Measurement of Thermal Expansion Coefficient of Flexible Substrate by Moiré Interferometry, *Exper. Techniques*, vol. 25, no. 3, pp. 22–25, 2001.
20. P. Kunthong, K. Verma, and B. Han, Effect of Underfill on C4 Bumps and Surface Laminar Circuit: An Experimental Study, *Proceedings of the 1999 IMAPS Conference*, Chicago, IL, October 1999.
21. B. Han and P. Kunthong, Micro-mechanical Deformation Analysis of Surface Laminar Circuit in Organic Flip-chip Package: An Experimental Study, *J. Elec. Packaging, Trans. ASME*, vol. 122, no. 3, pp. 294–300, 2000.
22. S. Cho and B. Han, Effect of Underfill on Flip-Chip Solder Bumps: An Experimental Study by Microscopic Moiré Interferometry, *Int. J. Microcircuits and Electronic Packaging*, vol. 24, no. 3, pp. 217–239, 2001.
23. M. Variyam and B. Han, DMD Module Calibration Using Interferometry, *TI Tech. J.*, pp. 1–8, 2001.
24. B. Han, Y. Guo, and H.-C. Choi, Out-of-plane Displacement Measurement of Printed Circuit Board by Shadow Moiré with Variable Sensitivity, *Proceedings of the 1993 ASME International Electronics Packaging Conference*, Binghamton, NY, September 1993.
25. C.-P. Yeh, I. C. Ume, R. E. Fulton, K. W. Wyatt, and J. W. Stafford, Correlation of Analytical and Experimental Approaches to Determine Thermally Induced PWB, *IEEE Trans. Components, Hybrids and Manufacturing Tech.*, vol. 16, no. 8, pp. 986–995, 1993.
26. Y. Guo, Applications of Shadow Moiré Method in Determination of Thermal Deformations in Electronic Packaging, *Proceedings of the 1995 SEM Spring Conference*, Grand Rapids, MI, 1995.
27. M. R. Stiteler, I. C. Ume, and B. Leutz, In-process Board Warpage Measurement in a Lab Scale Wave Soldering Oven, *IEEE Trans. Components, Packaging, and Manufacturing Tech. Pt. A*, vol. 19, no. 4, pp. 562–569, 1996.
28. D. B. Rao and M. Prakash, Effect of Substrate Warpage on the Second Level Assembly of Advanced Plastic Ball Grid Array (PBGA) Packages, *Proceedings of the 21st IEEE International Electronics Manufacturing Technology (IEMT) Symposium*, pp. 439–446, Oct. 13–15, Austin, TX, 1997.
29. K. Verma and B. Han, Warpage Measurement on Dielectric Rough Surfaces of Microelectronics Devices by Far Infrared Fizeau Interferometry, *J. Electronic. Packaging, Trans. ASME*, vol. 122, no. 3, pp. 227–232, 2000.
30. K. Verma, B. Han, S.-B. Park, and W. Ackerman, On the Design Parameters of Flip-Chip PBGA Package Assembly for Optimum Solder Ball Reliability, *IEEE Trans. Components and Packaging*, vol. 24, no. 2, pp. 300–307, 2001.
31. B. Han and D. Post, Immersion Interferometer for Microscopic Moiré Interferometry, *Exp. Mech.*, vol. 32, no. 1, pp. 38–41, 1992.
32. B. Han, Interferometric Methods with Enhanced Sensitivity by Optical/Digital Fringe Multiplication, *Appl. Optics*, vol. 32, no. 25, pp. 4713–4718, 1993.
33. B. Han, Higher Sensitivity Moiré Interferometry for Micromechanics Studies, *Opt. Engng.*, vol. 31, no. 7, pp. 1517–1526, 1992.
34. D. Post and J. Wood, Determination of Thermal Strains by Moiré Interferometry, *Exp. Mech.*, vol. 29, no. 3, pp. 318–322, 1989.
35. B. Han, D. Post, and P. Ifju, Moiré Interferometry for Engineering Mechanics: Current Practice and Future Development, *J. Strain Anal.*, vol. 36, no. 1, pp. 101–117, 2001.
36. S.-M. Cho, S. Y. Cho, and B. Han, Observing Real-Time Thermal Deformations in Electronic Packaging, *Exp. Techniques*, vol. 26, no. 3, pp. 25–29, 2002.

37. S.-M. Cho, J. Joo, and B. Han, Real-Time Moiré Interferometry for Deformation Analysis under Accelerated Thermal Cycling Condition, *Proceedings of IPACK'01*, July 2001, Kauai, HI. Also B. Han, S.-M. Cho, and J. Joo, Temperature Dependent Deformation Analysis of Ball Grid Array Package Assembly under Accelerated Thermal Cycling Condition, *J. Elec. Packaging, Trans. ASME*, in press, 2003.
38. Y. Tsukada, Solder Bumped Flip Chip Attach on SLC Board and Multi-chip Module, in J. H. Lau (ed.) *Chip on Board*, Ch. 9, pp. 410–443, Kluwer Academic, New York, 1994.
39. S. Ahan, Y. Kwon, and K. Shin, Popcorn Phenomenon in a Ball Grid Array Package, *Proceedings of the 44th IEEE ECTC*, pp. 1101–1107, Washington, DC, May 1994.
40. K. Verma and B. Han, Far Infrared Fizeau Interferometry, *Appl. Opt.*, vol. 40, no. 28, pp. 4981–4987, 2001.
41. B. Han, Optical Measurement of Flip-Chip Package Warpage and Its Effect on Thermal Interfaces, *Elec. Cooling*, vol. 9, no. 1, pp. 10–16, February 2003.
42. E. E. Marotta and B. Han, Thermal Control of Interfaces with Compliant Interstitial Materials for Microelectronics Packaging, *Proceedings of 1998 MRS Annual Spring Meeting*, San Francisco, CA, April 1998.